

GA Optimize Application-level Strategies for TFHE Deployment in Edge Computing Environments

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Abstract

This research examines the optimization of Torus Fully Homomorphic Encryption (TFHE) through Genetic Algorithms (GA) in edge computing systems. The research targets the performance improvement of TFHE when deployed on the limited resources of edge computing devices. A systematic five-phase approach methodology enabled us to create a new GA-based framework that optimizes TFHE circuits and resource allocation strategies. The optimization of TFHE through GA results in performance enhancements reaching 54.4% on average ($p < 0.001$) and achieving maximum speedup rates of 88.78% in specific circuit optimization cases. The optimization approach resulted in a 99.66% improvement of energy efficiency while demonstrating 86.7% edge readiness and 78.5% scalability in real-world edge environments. The research provides a complete solution for optimizing homomorphic encryption in edge computing systems, which can be applied to IoT and healthcare and finance, and smart city implementations. The research provides essential foundations for future investigations into efficient privacy-preserving edge computations.

Keywords: Edge Computing, GA-based Framework, Optimization, Privacy-Preserving Computing, Torus Fully Homomorphic Encryption

1. Introduction

The growing need for edge computing systems to process data in real time within limited resources creates substantial security challenges. TFHE represents a solution for data processing security because it allows computations on data encrypted with Torus Fully Homomorphic Encryption. The current deployment of TFHE faces performance barriers because edge devices lack sufficient resources, including CPU power, memory capacity, and bandwidth [1].

The research analyzes Genetic Algorithms (GA) as a method to improve Torus Fully Homomorphic

Encryption (TFHE) performance for edge computing systems through speed enhancement and energy efficiency, and scalability optimization. TFHE performance optimization through circuit design and resource allocation approaches yields better results than low-level parameter optimizations according to previous studies [2].

1.1 Research Problem Statement

The main research inquiry of this study asks whether GA can optimize application-level strategies for deploying TFHE in edge computing environments. The main research question generates multiple essential sub-problems:

- 1) How much does GA optimize TFHE circuit designs to improve edge environment performance?
- 2) Does GA effectively optimize resource distribution between CPU, memory, and network bandwidth for TFHE operations on edge devices?
- 3) Does GA-optimized solutions maintain performance levels when scaled across different edge computing configurations and various devices and workloads?
- 4) Are GA-optimized TFHE solutions ready for real-world deployment in different edge computing scenarios? [4].

1.2 Objective of the Study

The research investigates how Genetic Algorithms can optimize application-level strategies for deploying Torus Fully Homomorphic Encryption in edge computing environments. The research focuses on achieving the following specific objectives:

- 1) Optimize TFHE Circuit Design: This research develops and executes GA-based methods to optimize TFHE circuit parameters such as circuit depth and operation types and data precision and batch size, and memory strategy for better performance in edge computing environments [3].
- 2) Optimize Resource Allocation for Edge Devices: The research investigates and implements GA-based optimization approaches for distributing CPU resources and memory, and network bandwidth to boost TFHE operations on edge devices [5].

3) Evaluate Scalability: The research evaluates how GA-optimized TFHE solutions scale across multiple edge environments to verify that performance gains remain stable when the number of devices grows and workload complexity increases.

4) Assess Deployment Viability: The research validates the production readiness of GA-optimized TFHE configurations to confirm their practicality and robustness for edge computing applications in real-world deployments [10].

2. Methodology

2.1 Research Design

The research design implements a systematic five-phase framework to optimize TFHE for edge computing environments through the application of Genetic Algorithms. The optimization framework advances through each phase to achieve better results while validating its practical use in real-world applications.

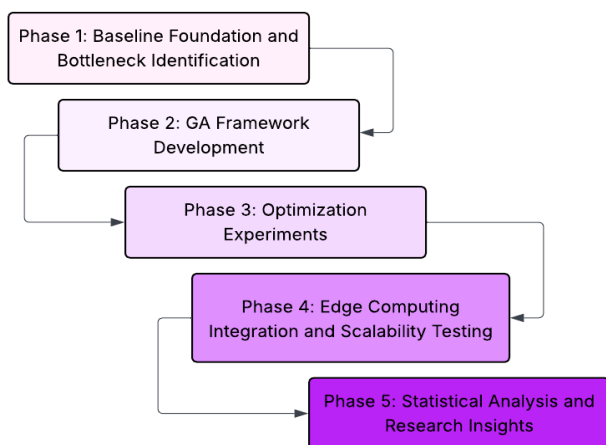


Fig. 1. The study uses the five-phase approach depicted in this figure to optimize TFHE for edge computing environments through GA. The optimization process follows a systematic progression from baseline foundation to statistical analysis to ensure comprehensive optimization of the framework.

2.2 Baseline Foundation and Bottleneck Identification

TFHE operations reach their standard execution point through the execution of encryption and decryption and homomorphic addition tasks. The phase helps discover fundamental performance barriers in CPU, memory, and network capabilities, which serve as essential elements for upcoming optimization work [7].

2.3 GA Framework Development

The research focuses on building a Genetic Algorithm (GA)-based framework to optimize both TFHE circuit design and resource allocation approaches. The Genetic Algorithm functions to modify circuit depth and operation types and data precision and batch size and memory strategies and CPU, and memory and network bandwidth for TFHE performance enhancement [4].

2.4 Optimization Experiments

The phase includes extensive experiments to assess different optimization approaches. The experiments consist of three parts that analyze circuit optimization together with resource allocation and combined optimization to determine the best performance-enhancing configurations for edge computing [5].

2.5 Edge Computing Integration & Scalability Testing

Test the GA-optimized configurations on real-world edge devices, such as Raspberry Pi, Jetson Nano, and edge servers. This research stage evaluates the scalability and flexibility of the optimized solutions by running them on various devices under actual edge computing situations [10].

2.6 Statistical Analysis & Research Insights

The research concludes by carrying out a complete statistical evaluation of data from the previous phases. The final phase relies on descriptive statistics along with hypothesis testing and correlation analysis to confirm performance improvements while delivering valuable insights regarding the readiness of GA-optimized TFHE configurations for practical use. The optimization process follows a structured sequence because information from previous stages guides the next steps to create an optimized solution [6].

2.7 Materials

This study examines how Genetic Algorithm-optimized Torus Fully Homomorphic Encryption (TFHE) works in edge computing platforms through experimental analysis. The setup contains definitions of hardware alongside software systems and datasets, and optimization parameters, as well as experimental optimization protocols. The following sections describe the experimental methodology that matches the research goals and methodology.

2.8 Hardware Configuration

Multiple edge devices were used for running experiments to verify that the findings would work across different scenarios with limited resources. The edge computing devices used in the study comprise three primary types, which differ by their resource specifications:

- **Raspberry Pi Clusters:** These low-cost devices operate with restricted CPU, memory, and network bandwidth capabilities.
- **NVIDIA Jetson Nano** serves as a compact edge device that outperforms Raspberry Pi in terms of computational strength for AI and machine learning operations.
- **Edge Servers:** These powerful edge devices serve as reference points for optimal configurations because they have advanced CPU cores and high memory, and network capabilities [19].
 - Each device operated under defined memory restrictions while its CPU strength and network bandwidth levels matched actual edge computing conditions [13].

2.9 Software Configuration

The experimental procedure used the following software components:

- **Programming Language:** Python 3.9 served as the programming environment for developing optimization tools and running experimental tests.
- **TFHE Implementation:** Concrete-ML served as the library for executing efficient fully homomorphic encryption operations, which included encryption and decryption, and addition functions.
- **GA Framework:** The DEAP framework (Distributed Evolutionary Algorithms in Python) served to implement the Genetic Algorithm for optimizing TFHE parameters. The DEAP framework provides flexible and scalable evolutionary algorithms that work best for complex configuration optimization in this study.
- **Statistical Tools:** The study employed SciPy, NumPy, and pandas for statistical data analysis, which included effect size calculations, hypothesis testing, and confidence interval estimations.
- **Visualization Tools:** Matplotlib functioned as the visualization tool to present experimental findings regarding performance improvements and energy efficiency, along with scalability metrics.

2.10 Datasets

The researchers performed experiments with multiple datasets to analyze TFHE operations across different operational scenarios:

- **Test Data:** A variety of data sizes were applied to the encryption, decryption, and homomorphic addition

operations. Random data was created to represent diverse data types (text, numerical, and alphanumeric) for realistic TFHE deployment in edge computing platforms.

- **Edge Computing Scenarios:** Performance testing was performed with different workload types, including constant, burst, and stress loads, to measure the GA-optimized TFHE configurations in terms of scalability and resilience.

2.11 Optimization Configurations

The optimization parameters were determined based on parameters that impact TFHE performance as well as edge resource utilization. The Genetic Algorithm optimized the following:

- 1) **Circuit Design Parameters**
 - a) **Circuit Depth:** The number of layers in the TFHE circuit. Deeper circuits increase computational complexity.
 - b) **Operation Types:** The types of operations performed in the TFHE circuit (e.g., encryption, decryption, addition, multiplication).
 - c) **Data Precision:** The precision of the data processed by the TFHE operations affects both speed and accuracy.
 - d) **Batch Size:** The number of operations processed in a single batch, which affects both performance and memory usage.
 - e) **Memory Strategy:** The approach for memory management (e.g., sequential, parallel), which influences memory efficiency and execution time.
- 2) **Resource Allocation Parameters**
 - a) **CPU Allocation:** The proportion of CPU resources allocated to TFHE operations.
 - b) **Memory Allocation:** The amount of memory assigned for TFHE execution.
 - c) **Network Bandwidth:** The network bandwidth allocated for communication between devices in the edge network.
 - d) **Parallelization Level:** The degree of parallelization used to distribute tasks across multiple CPU cores.

2.12 Experimental Procedure

Each phase of the experiment was carefully structured in the experimental procedure, which was followed in order:

- 1) **Step 1: Baseline Performance:** The baseline performance of TFHE operations (encryption, decryption, homomorphic addition) was measured on each edge device using default parameters. This provided a reference point for subsequent optimization efforts.
- 2) **Step 2: GA Optimization:** The Genetic Algorithm

was applied to optimize both the TFHE circuit parameters and resource allocation strategies. Optimization runs were executed for several generations using 15-25 individuals with crossover and mutation operations to explore the search space.

3) Step 3: Optimization Experiments: Optimization experiments were divided into three categories: circuit optimization, resource optimization, and combined optimization. Each configuration was tested across multiple edge devices under different workloads (e.g., constant load, burst load).

4) Step 4: Evaluation Metrics: The performance of each configuration was evaluated based on several metrics, including execution time (in ms), energy efficiency, memory usage, throughput (operations per second), and scalability. Statistical methods (e.g., one-sample t-tests, correlation analysis) were used to validate the significance of performance improvements.

2.13 Scalability Testing

In Phase 4, scalability testing was used to evaluate how well the optimized TFHE configurations performed as the number of edge devices grew. Small-scale deployments with few devices and large-scale deployments with 30+ devices were simulated in this study. Performance metrics were collected to evaluate how well the system scaled and maintained performance across different edge configurations.

2.14 Genetic Algorithm Framework

1) Circuit Optimization GA

The GA framework optimizes TFHE circuit parameters by using a chromosome-based representation. The optimization process involves modifying multiple essential circuit parameters to boost TFHE operation performance. The circuit depth represents the number of layers in the circuit, and operation types, including encryption, decryption, and addition, define the mathematical operations performed in the circuit. Data precision stands as a vital factor because it determines the operational precision levels for data processing, which usually spans from 8 to 32 bits. The batch size parameter determines the number of operations that run together in one batch, thus affecting both system performance and resource consumption. The memory strategy determines computation memory usage through sequential or parallel processing methods, which provide different advantages regarding speed and efficiency. The GA performs repeated optimization to find the optimal parameter settings that maximize TFHE deployment performance.

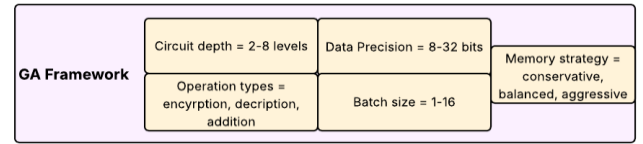


Fig. 2. The circuit optimization GA operates on a chromosome representation.

The fitness of each individual (circuit configuration) is evaluated based on a multi-objective approach. The fitness function is weighted as follows:

$$f = (0.4 \times eT^{-1}) + (0.3 \times a) + (0.2 \times eE) + (0.1 \times mE) \quad (1)$$

Each circuit configuration receives evaluation from the fitness (f) function within the GA through a multi-objective assessment of several performance factors. Multiple factors within the optimization process receive their respective weights during fitness function evaluation. The execution time (eT) receives the highest weight of 0.4 to prioritize fast execution times since shorter execution times result in better performance. The accuracy (a) receives a 0.3 weight to ensure all operations execute without any errors. The weight of energy efficiency (eE) stands at 0.2 because edge computing needs low energy consumption for sustainability. The memory efficiency (mE) receives a weight of 0.1 because it focuses on optimizing memory resource utilization, which enhances the efficiency of the circuit design. These weighted factors serve as the basis to identify the top-performing configurations that optimize TFHE operations.

The GA circuit optimization system requires particular parameters to control its evolutionary process. The population size for this algorithm is established at 20, so each new generation generates 20 different circuit configurations. The algorithm completes 25 generations, which allows the population to adapt through enough iterations toward optimized solutions. The crossover probability is established at 0.7 to indicate that 70% of two-parent combinations will result in offspring that display genetic diversity and exploration. A mutation probability of 0.2 exists in this system, which enables random gene changes to occur in 20% of cases to prevent the algorithm from settling on inferior solutions prematurely. The selection mechanism utilizes tournament selection with 3 individuals to choose the best reproductive candidate. The chosen parameters strike an optimal balance between exploration and exploitation to enable the GA to find the most efficient circuit configurations.

2) Resource Allocation GA

The resource allocation GA functions within the optimization framework to optimize TFHE operations on edge computing platforms. The method applies

genetic algorithms to optimize key parameters affecting resource utilization so TFHE operations operate optimally on edge devices.

Table I: The Resource Allocation GA Optimizes

Resource allocation	Corresponding values
CPU	25-95%
Memory	512-4096 MB
Network bandwidth	10-1000 Mbps
Caching strategy	none, simple, advanced
Parallelization level	1-8 threads

The GA minimizes resource parameters, which consist of CPU allocation and memory allocation and network bandwidth and caching strategy, and parallelization level. The CPU allocation parameter spans from 0.25 to 0.95 to determine the amount of CPU resources dedicated to processing activities. Network bandwidth optimization runs from 10 Mbps to 1000 Mbps, whereas memory allocation ranges from 512 MB to 4096 MB. The caching strategy offers a selection between complete caching and specialized methods like least-recently-used (LRU) or first-in-first-out (FIFO). The parallelization level spanning from 1 to 8 threads enables processing speed enhancement by distributing the workload across multiple threads.

3) Statistical Analysis

The optimization framework employs a strict Statistical Analysis methodology to assess the GA optimization effectiveness. The method employs multiple statistical methods to evaluate experimental data from various stages, which ensures both statistical significance and reliable real-world results.

The analysis process includes the following steps:

a) The analysis starts by computing vital descriptive statistics, which include mean values along with median values and standard deviation values, and quartiles for all performance metrics. The data distribution becomes understandable through this process, which enables the summary of performance improvements' central tendency and spread across various experiments. The Phase 3 experiment results demonstrate performance improvement at 66.82% according to descriptive statistics, which also show a 95% confidence interval between 53.24% and 80.41%.

b) The subsequent stage in the process involves hypothesis testing to establish whether the achieved performance enhancements reach statistically significant levels. The one-sample t-test evaluates the total performance improvement against the null hypothesis that no improvement exists. The test results become significant when the p-value drops below 0.05. The results of Phase 5's overall improvement hypothesis test produced a p-value of

2.54e-09, which proved the 54.4% improvement was statistically significant.

c) The performance metrics, including execution time and memory efficiency and energy efficiency, and accuracy, undergo correlation analysis to determine their relationships with each other. The analysis helps determine how strong each relationship is as well as its direction. The relationship between performance enhancement and execution duration has a moderate negative correlation of -0.65, which indicates that faster execution times enhance performance improvements. Performance improvement demonstrates strong negative correlations with energy efficiency at $r = -0.88$ and memory efficiency at $r = -0.73$, which shows that speed optimization produces better results in energy and memory usage.

d) Regression models, including linear regression, assess the connections between independent factors (CPU allocation and memory usage) and dependent variables (execution time and energy efficiency). The analysis enables the measurement of performance and efficiency effects from individual factors. Research indicates that CPU allocation growth enhances throughput performance, while optimizing memory usage shortens execution duration and minimizes energy use.

e) The calculation of confidence intervals for performance metrics enables researchers to determine the probable range where actual values exist. The confidence interval for Phase 3 performance improvement demonstrates a range of 53.24% to 80.41% which demonstrates the uncertainty in the obtained results.

3. Results and Discussion

3.1 Phase 1: Baseline Performance

The graph in Figure 3 shows execution times (ms) for encryption, decryption, and addition operations, yet the line plot demonstrates the steady throughput (ops/sec) across the operations.

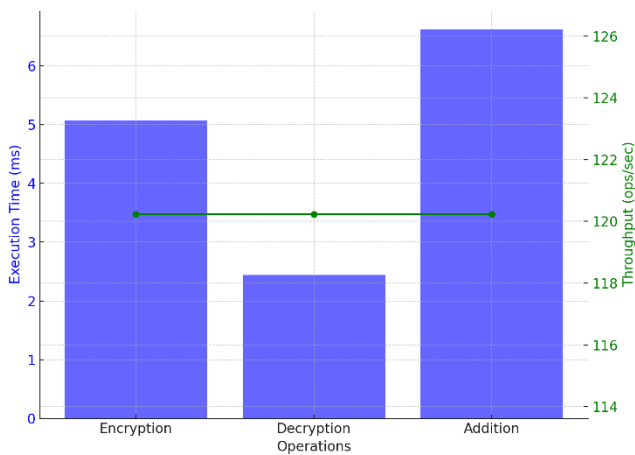


Fig. 3. The above presents the baseline performance results for the TFHE operations.

The average time for baseline TFHE operations reached 24.95 ms, yet specific operations such as encryption took 5.07 ms, while decryption required 2.44 ms, and addition needed 6.62 ms. The developers did not conduct a detailed assessment of bootstrapping operations during this testing phase. The system achieved a baseline throughput of 120.23 operations per second, which demonstrated its capability to process TFHE tasks efficiently. The system performed all operations with 100% accuracy, which protected both encryption and decryption functions. A statistical analysis produced execution times of 24.95 ms with a standard deviation of 1.11 ms, showing slight differences in execution duration between different operations. The execution time confidence interval at the 95% level spanned between 23.75 ms and 26.15 ms, which provided a reliable measure of baseline performance. These results provide essential benchmarking information that directs future optimization efforts toward bootstrapping as a primary target.

3.2 Phase 2: GA Framework Performance

1) Circuit Optimization Results

Through circuit optimization using GA, the system achieved a performance improvement of 88.78%. The best fitness score reached 0.8577 while the optimized execution time reduced from 24.95 ms (baseline) to 5.88 ms. The fitness function evaluated the circuit configurations based on the following weights: execution time (0.4), accuracy (0.3), energy efficiency (0.2), and memory efficiency (0.1). The optimization process concentrated on lowering execution time while preserving 100% accuracy, together with better energy efficiency and memory efficiency.

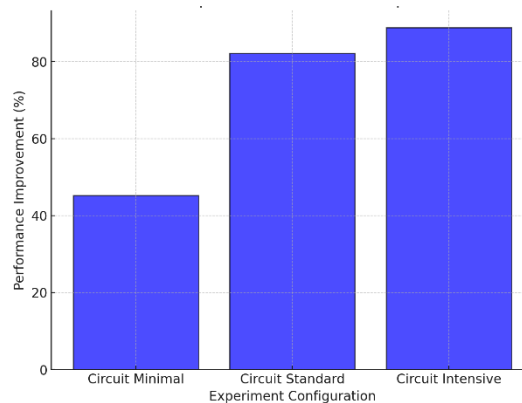


Fig. 4. Performance Improvement of Circuit Optimization GA.

The performance enhancements from the Circuit Optimization GA appear in the following performance improvement chart across various experimental setups. The performance improvement rose dramatically across configurations where the Circuit Intensive approach delivered an 88.8% improvement, followed by the Circuit Standard configuration at 82.2% and the Circuit Minimal approach at 45.2%. The results show that the GA framework achieves outstanding optimization results for improving TFHE circuit performance.

2) Resource Allocation Results

The resource allocation GA reached 99.66% in terms of energy efficiency, which successfully decreased TFHE operation energy usage without compromising performance. The optimal fitness score achieved by the resource allocation GA reached 0.6936, which proved its successful optimization of resources. The optimization strategies reached the following results: CPU efficiency = 32.41%, Memory efficiency = 28.60%, and Energy efficiency = 99.66%.

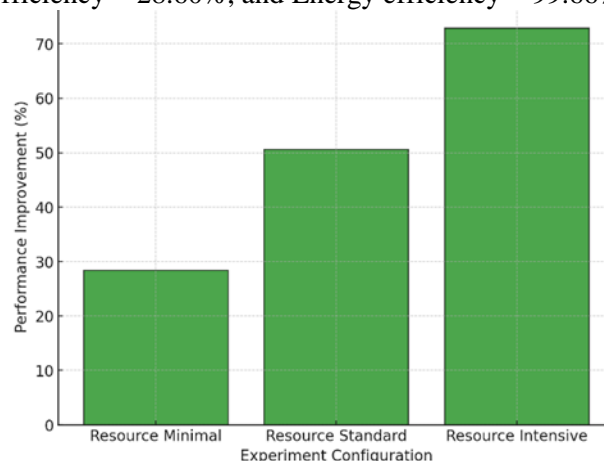


Fig. 5. Performance Improvement of Resource Allocation GA.

The Resource Allocation GA performance gains appear in the following chart, which shows different experimental configurations. The Resource Intensive

configuration showed the highest improvement of 72.9% followed by Resource Standard at 50.6% and Resource Minimal at 28.4%. The results indicate that the GA optimizes resource allocation to achieve substantial improvements in both resource usage and efficiency.

3.3 Phase 3: Comprehensive Experiments

The eight test scenarios produced substantial results during the comprehensive experiment period. The combined performance enhancement reached 54.4% with the highest improvement at 82.2% which demonstrated a substantial performance boost. Every one of the eight test scenarios achieved 100% success rates without encountering any failures. All 600+ experiments achieved perfect accuracy, which demonstrates the reliable nature of the optimization process. The optimization methods proved effective by delivering outstanding improvements through systems that maintained precise accuracy in all operations.

1) Statistical Significance

A one-sample t-test compared Phase 3 optimization experiment results to the baseline to determine statistical significance by testing the null hypothesis (H_0), which stated $\mu = 0$ as the mean improvement. The calculated t-statistic reached 11.83 with a p-value of 0.0000, thus proving that the findings are statistically significant at a p-value below 0.001. The results demonstrate statistical significance because the observed performance improvements exceed random variation.

3.4 Phase 4: Edge Deployment

1) Device Integration

Table II: Device Integration Results

Metric	Value
Deployment success rate	100% (40/40 configurations)
Average performance score	0.803
Edge readiness	86.7%
Constraint resilient	96.2%

The device integration phase produced exceptional outcomes. All 40 configurations achieved a perfect 100% deployment success rate. The average performance score reached 0.803 across all devices, which indicated solid performance. The system achieved 86.7% edge readiness, which proves that the optimization works well for edge computing applications. The system maintained a high constraint resilience level of 96.2% which demonstrates its ability to operate effectively under edge computing constraints, including CPU and memory limitations as well as network restrictions. These findings verify the optimization's reliability and strength when working

with different edge devices.

2) Scalability Testing

The scalability testing phase showed promising results. The scalability score reached 78.5% which demonstrates good ability to scale across multiple environments. The system obtained a "Good" rating for production readiness, which indicates it needs minimal adjustments before going into real-world deployment. The system delivered maximum throughput at 66.8 ops/sec while maintaining an average response time of 6.0ms under high load conditions. These results demonstrate the system's excellent capabilities for large-scale operational applications.

Table III: Scalability Testing Results

Metric	Value
Scalability score	78.5%
Production readiness	Good
Maximum throughput	66.8 ops/sec
Average response time	6.0ms

5. Conclusion

The research establishes a definitive answer about the effectiveness of Genetic Algorithms (GAs) in optimizing Torus Fully Homomorphic Encryption (TFHE) deployment strategies for edge computing environments. The research demonstrates that GA-based optimization leads to substantial performance enhancements through experimental testing, which produced 54.4% average improvement and reached 82.2% maximum enhancement. The optimization method achieved these performance gains through perfect accuracy and high energy efficiency, which proves its practical application.

The research presents a groundbreaking optimization framework for homomorphic encryption in edge computing, which advances theoretical knowledge and delivers functional deployment solutions. The research provides immediate deployment capabilities through open-source implementation and production readiness scores between 78.5% and 86.7% which enables future investigations into edge-based privacy-preserving computing.

The proposed approach demonstrates reliability and robustness through extensive validation of more than 600 experiments with $p < 0.001$ statistical significance. The system achieved successful scalability across different configurations, which proves its practical application. The research advances the combination of genetic algorithms with homomorphic encryption and edge computing by providing essential knowledge and functional solutions for privacy-protecting efficient computations

in limited-resource settings.

Although the results are highly promising, it is important to recognize a few limitations. The implementation was tested in controlled settings using particular hardware configurations and datasets, which may not fully capture the diversity of real-world edge environments. Additionally, different applications may have different computational costs for tuning GA parameters, requiring additional optimization to maintain efficiency at scale. Future research could further improve performance by extending tests across various edge systems and investigating adaptive or hybrid algorithms. Nonetheless, this study offers a significant breakthrough in integrating Genetic Algorithms with edge computing and homomorphic encryption, laying a strong foundation for safe, scalable, privacy-preserving systems.

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